REMARKS

The present paper is submitted in response to the Examiner's Final Office Action mailed July 25, 2008. No claims are amended. Claims 1-40 remain pending.

Reconsideration of the application is respectfully requested in view of the following remarks. For the Examiner's convenience and reference, Applicant's remarks are presented in the order in which the corresponding issues were raised in the Office Action.

I. GENERAL CONSIDERATIONS

Applicants note that the remarks, or a lack of remarks, set forth herein are not intended to constitute, and should not be construed as, an acquiescence, on the part of the Applicants: as to the purported teachings or prior art status of the cited references; as to the characterization of the cited references advanced by the Examiner; or as to any other assertions, allegations or characterizations made by the Examiner at any time in this case. Applicants reserve the right to challenge the purported teaching and prior art status of the cited references at any appropriate time.

II. REJECTION UNDER 35 U.S.C. § 112, First Paragraph

The Examiner rejected claim 40 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Claim 40 recites, among other things, "interspersing a bit at a guaranteed minimum frequency." According to the Examiner "There is no support for guaranteeing at a minimum frequency." *See Office Action*, p. 2. Applicants respectfully disagree.

"The examiner has the initial burden of presenting evidence or reasoning to explain why persons skilled in the art would not recognize in the original disclosure a description of the invention defined by the claims." *MPEP* § 2163.II.A.3.(b). "To satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention." *MPEP* § 2163.I. *See also* § 2163.02 ("The subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement.")

Applicants respectfully submit that the Examiner has not met the initial burden of presenting evidence or reasoning to explain why persons skilled in the art would not recognize in the original disclosure a description of the invention defined by claim 40. In particular, the

Examiner has merely alleged, "There is no support for guaranteeing at a minimum frequency." *See Office Action*, p. 2. Conclusory statements of this type do not constitute "evidence or reasoning."

Moreover, contrary to the Examiner's conclusory assertion, the specification describes "interspersing a bit at a guaranteed minimum frequency" in sufficient detail to satisfy the written description requirement. For example, paragraph [0035] of the specification states that "[a] frame 200 is designed so that within any component's turn for control of the data wire, there is a guaranteed zero interspersed more frequently than the length of the preamble." One skilled in the art would have recognized that interspersing a zero more frequently than the length of a preamble is an example description of the claimed "interspersing a bit at a guaranteed minimum frequency."

Further written description support may be found, for example, at paragraphs [0042] and [0043] of the specification. Paragraph [0042] states that "[a] frame is designed such that neither a master nor a slave transmits more than fifteen consecutive logical ones in a row when transmitting [non]-preamble portions of the frame." Paragraph [0043] then states that no more than fifteen consecutive logical ones in a row are transmitted "due to the interspersed guaranteed zeros within the frame design." One skilled in the art would have recognized that interspersing a zero such that no more than fifteen consecutive logical ones in a row are ever transmitted during non-preamble portions of a frame is another example description of the claimed "interspersing a bit at a guaranteed minimum frequency."

Further written description support may be found, for example, at paragraph [0080] of the specification, which states that "bits are interspersed throughout [a] frame such that it is guaranteed that there will never be the predetermined number of consecutive bits representative of the preamble on the data wire if another component is transmitting another portion of a frame on the data wire." One skilled in the art would have recognized that interspersing a bit throughout a frame in this manner is another example description of the claimed "interspersing a bit at a guaranteed minimum frequency."

Figures 3A, 3B, and 3C also provide written description support for "interspersing a bit at a guaranteed minimum frequency." For example, in describing Figure 3A, paragraph [0058] of the specification states, "The master component then transmits a guaranteed logical zero as bit 42 thereby ensuring that fifteen consecutive logical ones on the data wire 132 means that a frame is

in the preamble phase...." Other guaranteed zero bits are also described, for example, in paragraphs [0065] ("bit 23") and [0067] ("bit 14").

In light of the foregoing examples of written description support and because the Examiner has failed to meet the initial burden for establishing lack of written description support, Applicants respectfully submit that the rejection of claim 40 is improper and should be withdrawn. Should the Examiner continue to maintain the rejection under 35 U.S.C. § 112, first paragraph, **Applicants respectfully request that sufficient "evidence or reasoning" be provided** to explain why persons skilled in the art would not recognize the original disclosure as providing written description support for claim 40.

III. REJECTION UNDER 35 U.S.C. §102(b)

The Examiner rejected claims 1-5, 8-10, 12, 13, 23-26, and 28-30 under 35 U.S.C. § 102(b) as being anticipated by *Creedon et al.* (U.S. Patent No. 6,385,669). Because *Creedon* does not describe each and every element of the rejected claims, Applicants respectfully traverse the rejection in view of the following remarks.

In the Office Action, the Examiner made a variety of characterizations of *Creedon*, at least three of which Applicants have been able to identify as separate characterizations. Each of these characterizations is discussed in turn below. Because the separate characterizations are not clearly identified by the Examiner, clarification is respectfully requested if the number of characterizations is believed to differ or if Applicants' understanding of a characterization is inaccurate.

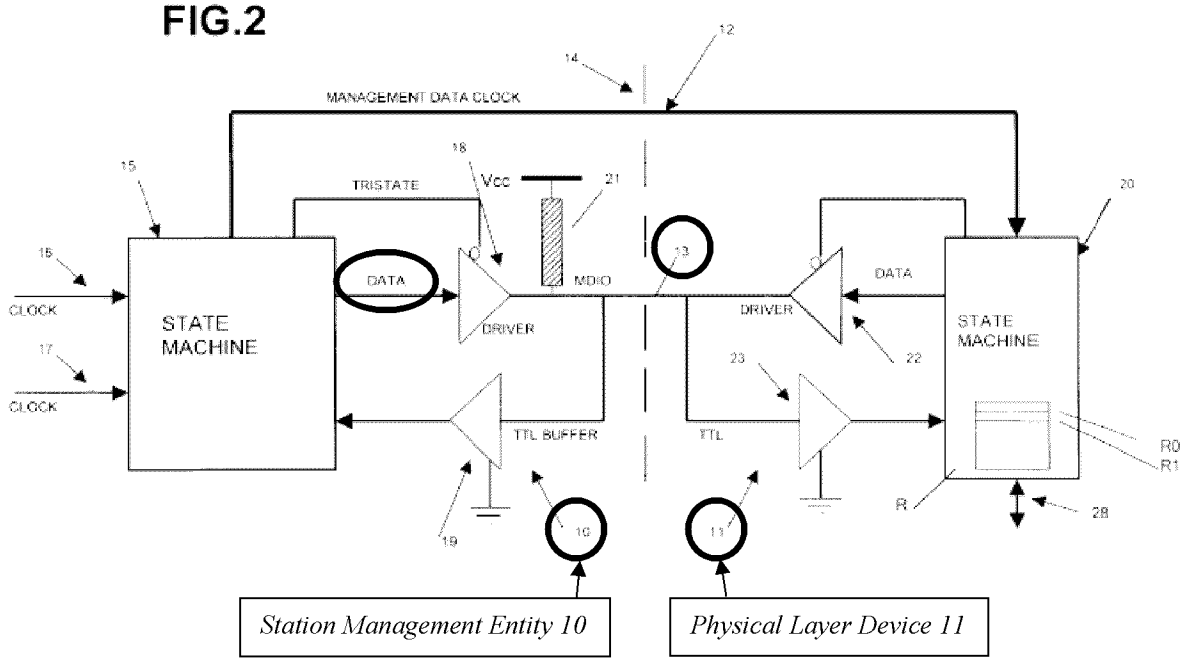
A. First Characterization of *Creedon*

In the "Claim Rejections" section of the Office Action, the Examiner alleged that the monitoring and detecting limitations recited in each of claims 1, 23, and 28 read on column 4, lines 60-67 of *Creedon*, which describes a frame preamble. *See Office Action*, pp. 3, 4, and 5. The rejection is repeated almost verbatim from the previous two Office Actions. However, as noted in Applicants' previous responses filed on December 10, 2007 (*see* pages 10 and 11), and on April 25, 2008 (*see* pages 15 and 16), the Examiner's characterization of *Creedon* implies that the station management entity 10 monitors and detects its own preamble, which is not described anywhere in *Creedon* and therefore mischaracterizes *Creedon*.

In the most recent Office Action, the Examiner responded to the foregoing points by asserting that entity 10 does not send a preamble. *See Office Action*, p. 8 ("[S]ince the default

logic [of line 13] is one, the management entity is not sending any information as argued by Applicant.") However, **the Examiner continues to mischaracterize *Creedon*** in asserting that "the management entity is not sending any information" simply because line 13 purportedly has a default logic state of one. The Examiner's characterization is plainly contradicted at least in Figure 2, which depicts data being sent by entity 10 over line 13. (See annotated copy of Figure 2 below.)

FIG.2



In describing Figure 2 *Creedon* states, "The management entity [10] includes a state machine 15 which...provides a serial data signal in a specified frame format to...the management data input/output bus line 13." *See* col. 3, line 65, through col. 4, line 12. In addition, according to *Creedon*, entity 10 uses line 13 for "conveying frames to the physical layer device 11." *See id.* Therefore, the Examiner's assertion that "the management entity is not sending any information" is a **mischaracterization of *Creedon***.

B. Second Characterization of *Creedon*

In the "Response to Arguments" section of the Office Action, the Examiner characterized *Creedon* in another way. In particular, the Examiner alleged that the monitoring and detecting limitations read on column 4, lines 43-44, which purportedly describes a default voltage level on a bus line 13. *See Office Action*, pp. 8 and 9 ("Creedon discloses the act of monitoring for at

least a predetermined number of consecutive bits of the same binary polarity (i.e. Logic one, which is the default logic [of line 13] caused by [a] pull up resistor)."

However, as noted in Applicants' previous response filed on April 25, 2008 (*see* page 16), *Creedon* describes determining a voltage level of line 13 "at controlled times." *See* col. 4, lines 17 and 18 (emphasis added). In contrast each of claims 1, 23, and 28 recites "monitoring the data wire of the two-wire interface upon determining that the operation is to be performed on the slave component." (Emphasis added.)

While this shortcoming in the rejection was clearly identified in Applicants' paper filed April 25, 2008, the Examiner has nonetheless failed to respond, in the Office Action mailed July 25, 2008, to the points advanced by Applicants in that paper. The failure of the Examiner to address Applicants' prior arguments is contrary to established examination guidelines. Particularly, Applicants note that "[w]here the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, **take note of the applicant 's argument and answer the substance of it**." *See MPEP* § 707.07(f) (emphasis added).

C. Third Characterization of *Creedon*

The Examiner's third characterization of *Creedon* also appeared in the "Response to Arguments" section of the Office Action. The Examiner alleged that certain techniques described in paragraphs [0042] and [0043] of Applicants' specification are "used by applicant's method to monitor and detect consecutive bits" and that "[t]his is the same as the Creedon's method for monitoring and detecting the consecutive bits." Applicants respectfully disagree.

The Examiner has not established, beyond mere allegation, either of the following: 1) that the techniques in paragraphs [0042] and [0043] must be "used by" the claimed method, or 2) that the claimed method "is the same as" anything described by *Creedon*. In fact, *Creedon* teaches that "a management frame…is conveyed…when the state machine requires to perform either a write operation or a read operation on…device 11." *See* col. 4, lines 58-62. In sharp contrast, each of claims 1, 23, and 28 recites "monitoring the data wire…upon determining that [an] operation is to be performed on [a] slave component; [and] detecting at least a predetermined number of consecutive bits…while monitoring the data wire."

Moreover, the sweeping assertion that "applicant's method…is the same as the Creedon's method" is **not supported by substantial evidence** at least inasmuch as the Examiner has not cited any particular teaching in *Creedon* to support the assertion. Therefore the Examiner has

failed to establish, beyond mere allegation, that the claims are anticipated under 35 U.S.C. § 102(b). *See MPEP* § 2144.03 ("The standard of review applied to findings of fact is the 'substantial evidence' standard under the Administrative Procedure Act (APA).") (citing *In re Gartside*, 203 F.3d 1305, 1315 (Fed. Cir. 2000)). With regard to the foregoing, Applicants further note in general that "[t]he goal of examination is to **clearly articulate any rejection** early in the prosecution process so that the applicant has the opportunity to provide evidence of patentability and otherwise reply completely at the earliest opportunity." *See MPEP* § 706 (emphasis added).

In view of the foregoing remarks regarding each of the *Creedon* characterizations, Applicants respectfully submit that the Examiner has failed to establish that *Creedon* anticipates any one of claims 1, 23, or 28, at least because the Examiner has not established that each and every element as set forth in the claims is found in *Creedon*, and because the Examiner has not established that the identical invention is shown in *Creedon* in as complete detail as is contained in the claims. Applicants thus respectfully submit that the rejection of claims 1, 23, and 28, and corresponding dependent claims 2-5, 8-10, 12, 13, 24-26, 29, and 30, should be withdrawn.

D. Further Remarks

Each of claims 1, 23, and 28 recites "asserting a frame of the two-wire interface on the data wire in response to detecting that the predetermined number of consecutive bits of the same polarity have occurred on the data wire." The Examiner identified a start of frame section of the frame format in Figure 4 as the claimed "frame," asserting that *Creedon* implicitly teaches the start of frame section "is in response to detecting consecutive bits since the frame format requires a preamble of 32 consecutive bits. Again, **if** the required consecutive ones are not observed, **then** the preamble phase has not been satisfied. Therefore, start frame is only send **after** the required consecutive ones are detected." *See Office Action*, p. 9 (emphasis added). Applicants respectfully disagree.

The Examiner asserted that the start frame is sent as a result of (i.e., "**if…then**") a detection of the preamble or "**after**" observation of the preamble. However, no such conditional relationship is described by *Creedon*. Instead, the start of frame section is sent **regardless** of whether any preamble bits are observed or detected. *See Creedon*, Figure 4 and col. 5, line 7 ("The next portion of the frame format [after the preamble] is a start of frame ST.") Therefore, should the Examiner continue to assert that sending the start of frame section is sent **conditioned**

on the preamble bits being "detected" or "observed," Applicants respectfully request a detailed explanation of where such conditions are described in *Creedon*, particularly in light of Figure 4 and column 5, line 7, of *Creedon*.

Therefore, Applicants respectfully submit that the rejection of claims 1, 23, and 28, and corresponding dependent claims 2-5, 8-10, 12, 13, 24-26, 29, and 30, should be withdrawn for at least these additional reasons.

IV. REJECTION UNDER 35 U.S.C. §103

The Examiner rejected claims 6, 7, 11, 14-22, and 31-40 under 35 U.S.C. § 103 as being unpatentable over *Creedon et al.* (U.S. Patent No. 6,385,669) in view of what is purportedly "well known in the art."

Applicants note that inasmuch as the rejection of claims 6, 7, 11, 14-22, and 31-39 relies on the characterization of *Creedon* advanced by the Examiner in connection with the rejection of claims 1 and 28, the rejection of claims 6, 7, 11, 14-22, and 31-39 lacks an adequate basis for at least the reasons set forth in the discussion at section III above. Accordingly, the attention of the Examiner is respectfully directed to such discussion. For example, it was noted in such discussion that the Examiner has failed to establish that *Creedon* teaches all the limitations of claims 1 and 28, from which claims 6, 7, 11, 14-22, and 31-39 depend. Thus, Applicants respectfully submit that it is clear that even if the references are combined, the resulting combination fails to include all the limitations of claims 6, 7, 11, 14-22, and 31-39.

Applicants further submit that the rejection of claim 40 under section 103 should be withdrawn for additional reasons. Claim 40 recites: "interspersing a bit at a guaranteed minimum frequency among data transmitted on the data wire, wherein the interspersed bit is of a polarity opposite that of the detected predetermined number of consecutive bits." Although, according to the Examiner, *Creedon* fails to specifically disclose the aforementioned claim limitations, the Examiner alleged that "[i]t would have been obvious to...use zero stuffing...." *See Office Action*, pp. 7 and 8.

Applicants respectfully submit, however, that "zero stuffing" (alternatively referred to as "bit stuffing") is not equivalent to "interspersing a bit at a guaranteed minimum frequency among data...," as claimed. (Emphasis added.) Rather, bit stuffing, as defined in the reference cited by the Examiner, is "[t]he practice of adding bits to a stream of data." The definition also cites a variety of "reasons" that bit stuffing can be required, but does not describe, either

explicitly or implicitly, "interspersing a bit at a guaranteed minimum frequency," as claimed. (Emphasis added.)

CONCLUSION

In view of the foregoing, Applicants believe the claims are in allowable form. In the event that the Examiner finds remaining impediment to a prompt allowance of this application that may be clarified through a telephone interview, or which may be overcome by an Examiner's Amendment, the Examiner is requested to contact the undersigned attorney.

The Commissioner is hereby authorized to charge payment of any of the following fees that may be applicable to this communication, or credit any overpayment, to Deposit Account No. 23-3178: (1) any filing fees required under 37 CFR § 1.16; and/or (2) any patent application and reexamination processing fees under 37 CFR § 1.17; and/or (3) any post issuance fees under 37 CFR § 1.20. In addition, if any additional extension of time is required, which has not otherwise been requested, please consider this a petition therefor and charge any additional fees that may be required to Deposit Account No. 23-3178.

Dated this 23rd day of September, 2008.

Respectfully submitted,

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